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Modulating the Interface Quality and Electrical Properties of HfTiO/InGaAs Gate Stack by Atomic-Layer-Deposition-Derived Al_2O_3 Passivation Layer

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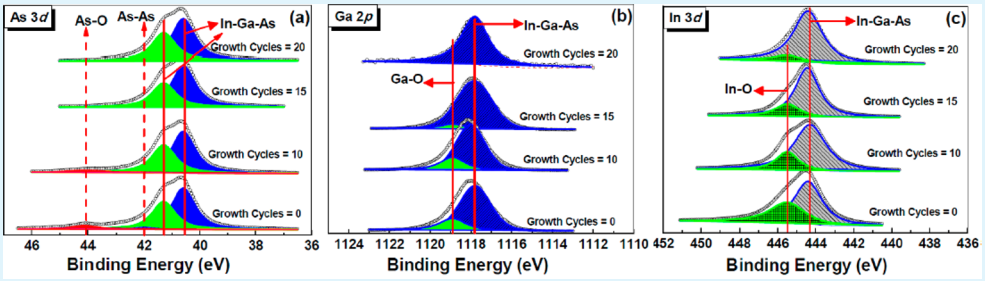
Supporting Information



ABSTRACT: In current work, the effect of the growth cycles of atomic-layer-deposition (ALD) derived ultrathin Al_2O_3 interfacial passivation layer on the interface chemistry and electrical properties of MOS capacitors based on sputtering-derived HfTiO as gate dielectric on InGaAs substrate. Significant suppression of formation of Ga−O and As−O bond from InGaAs surface after deposition of ALD Al_2O_3 with growth cycles of 20 has been achieved. X-ray photoelectron spectroscopy (XPS) measurements have confirmed that suppressing the formation of interfacial layer at HfTiO/InGaAs interface can be achieved by introducing the Al_2O_3 interface passivation layer. Meanwhile, increased conduction band offset and reduced valence band offset have been observed for HfTiO/Al_2O_3/InGaAs gate stack. Electrical measurements of MOS capacitor with HfTiO/Al_2O_3/InGaAs gate stacks with dielectric thickness of ∼4 nm indicate improved electrical performance. A low interface-state density of (∼1.9) × 10^{12} eV^{-1} cm^{-2} with low frequency dispersion (∼ 3.52%), small border trap density of 2.6 × 10^{12} cm^{-2}, and low leakage current of 1.17 × 10^{-5} A/cm^2 at applied gate voltage of 1 V have been obtained. The involved leakage current conduction mechanisms for metal-oxide-semiconductor (MOS) capacitor devices with and without Al_2O_3 interface control layer also have been discussed in detail.

KEYWORDS: *high-k gate dielectric, atomic-layer-deposition, metal-oxide-semiconductor, surface passivation, electrical properties*

1. INTRODUCTION

Requirements for devices with high speed and low power consumption have pushed Si-based metal-oxide-semiconductor field-effect-transistor (MOSFET) to scale down to their limit. Currently, III−V semiconductors with high mobility are being paid more attention as one of the promising technology boosters which can improve the MOSFET performance not only by relying on scaling. Among III−V semiconductor, $In_{1-x}Ga_xAs$ and InP have been chosen as alternative channel material to Si to extend the MOSFETs' performance limits owing to their higher carrier mobility and smaller effective mass compared to those of Si or strained Si.[1−3] To obtain gate capacitance with good scalability, high-*k* dielectrics, such as HfO_2 and its derivatives, are deposited on III−V semiconductor substrates, such as GaAs and InGaAs.[4,5]

However, III−V semiconductors maybe form extrinsic defects and high interface state density (D_{it}) due to the existence of native oxides. The high D_{it} attributed to the interface of dielectric/III−V leads to the production of Fermi level pinning, which prevents the formation of inversion or accumulation layer and degrades the drive current and the subthreshold swing.[6] The removal of surface species is confirmed to be effective to unpinning the Fermi level.[7,8] Therefore, different surface-passivation techniques of III−V substrates upon gate stack formation have been intensively explored. For instance, depositing a Si or Ge thin layer prior to high-k gate dielectric deposition has been confirmed to be effective to improve the quality of interface.[9−11] However, it can be noted that Ge and Si can act as amphoteric dopants in GaAs, a Si or Ge thin layer may change the doping content or

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even lead to the counter doping of the GaAs substrate, attributing to the instability of the threshold voltage.[12] Moreover, Si, Ge, control layers thicken the high-k gate dielectric, reducing the dielectric constant of the gate dielectric thus hindering oxide physical thickness scaling to a acceptable range.[1] In addition, wet chemical processing,[13,14] atomic hydrogen treatments,[15] as well as sulfur[16] and nitrogen passivations[17] have all been employed to move away native oxides and diminish the interaction between any deposited oxide and the semiconductor. However, although these processes have shown improvements in device performance, the D_{it} levels are still too high to make the incorporation of a III−V channel as a viable alternative to Si in the short term.

Fortunately, current progress of direct depositing high-k gate dielectrics has realized the possibility of fabricating III−V-based CMOS devices, solving its poor interface quality problems.[18,19] Owing to the good thermal stability and appropriate band alignment, HfO_2 high-k gate dielectric has been investigated for scaled InGaAs MOSFETs.[20] However, their moderate dielectric constants make Hf-based gate dielectrics limited for future CMOS device scaling.[21]Currently, more attention has been paid to investigate the TiO_2-incorporated HfO_2 high-k gate dielectrics because of its adjustable dielectric constant, good thermal stability, and excellent electrical properties in MOS devices.[22−24] Similar to other high-k gate dielectrics, direct deposition of HfTiO gate dielectrics on InGaAs also exhibits anomalous characteristics with larger frequency dispersion, hysteresis, and also low effective mobility, originating from the native oxides derived Fermi level pining.[21] Therefore, the pretreatment and the passivation of the InGaAs substrate prior to depositing high-k gate dielectric to reduce the formation of the oxides and exclude the Fermi level pinning is still necessary.[21]However, these methods introduce more complicated operating procedure and degrade the device performance. The development of alternative passivation process for InGaAs surface is desirable. More recently, with atomic-layer-deposited (ALD) high-k gate dielectrics on InGaAs substrates, an native-oxide-free interface has been detected.[25,26] This case can be attributed to the self-cleaning effect of ALD Al_2O_3 or HfO_2, which reduces the native oxide from the substrate surface.[8,27]Although progress on self-cleaning effect at high-k/III−V interface has been made, the understanding of the self-cleaning mechanism is still limited. Especially, for sputter oxide dielectric growth on III−V substrates, ALD Al_2O_3 surface passivation for substrate is very important to remove native oxide of substrate surface to avoid Fermi level pinning in III−V-based MOS devices. As we know, for sputtered oxides growth on III−V substrates, formation of thick interfacial layer has been observed, which leads to the degreased electrical performance in III−V based devices. Therefore, the reduction and suppressed interfacial layer between III−V substrate and high-k gate dielectrics should be desirable.[21,23,24] In current repor t, prior to the sputtering-derived HfTiO gate dielectric, ALD-derived aluminum oxide (Al_2O_3) control layer for InGaAs and its application in HfTiO-InGaAs gate stacks has been investigated systematically. By far, there exist some investigations on the electrical performance of HfO_2/InGaAs gate stack with interface passivation layer,[27] few observation on the evolution of the interface chemistry of HfTiO/InGaAs gate stacks, as well as the band alignment and electrical properties of the HfTiO/InGaAs, originating from the effective passivation of InGaAs surface by ALD-derived Al_2O_3 passivation layer with self-cleaning effect, has not been fully identified yet. As we know, ALD Al_2O_3 can effectively remove the native oxides of the substrate surface. However, the disappearance of the native oxide is determined by the ALD chemical reactions at an InGaAs surface, which is affected by the ALD temperature and the ALD growth cycles. For the ALD-determined surface evolution, the self-cleaning effect of high-k/InGaAs system as a function of ALD temperature has also been investigated.[20] However, no related observations on the effect of ALD growth cycles on the Al_2O_3/InGaAs interface chemistry has been reported. In addition, the illumination and understating of self-cleaning effect of ALD Al_2O_3 gate dielectrics related with ALD growth cycles play an important role in constructing III−V-based MOSFET. As a result, the effect of ALD growth cycles on the Al_2O_3/InGaAs interface has been investigated to understand the factors to determine the interfacial properties, band alignment and electrical properties of HfTiO/InGaAs gate stacks in current work.

2. EXPERIMENTAL SECTION

2.1. Samples Preparation and MOS Fabrication. Commercially available n-type Si-doped InGaAs wafers with a doping concentration of $\sim 10^{17}$ cm^{-3} were used as substrates in this work. Before transferring the substrates to the ALD chamber, all the substrates were degreased by dipping in acetone, methanol, and isopropyl alcohol for 1 min each to remove the organic matters and other impurity ions and remained native oxide layer adhered to the surface of the substrates. Then, all wafers were followed by rinsing in deionized water and drying by N_2. After that, these wafers were transferred into ALD chamber (LabNano 9100, ENSURE NANOTECH). Al_2O_3 passivation layer was grown on the as-processed InGaAs substrate, using trimethylaluminum [Al-$(CH_3)_3$, (TMA)] and H_2O and as the metal precursor and oxidant, respectively. TMA was contained in bubbler at room temperature and transferred to the reaction chamber by N_2 with high purity. Experimental ALD pulsing sequence is TMA (0.5s)/N_2 purge (2.0s)/H_2O (0.5s)/N_2 purge (2.0s) for the growth of Al_2O_3 passivation layer. During deposition, the chamber base pressure and the growth temperature were ∼1.0 Torr and 200 °C, respectively. To investigate the growth cycles dependent surface chemistry of the InGaAs substrate, the growth cycles for Al_2O_3 layer are fixed at 10, 15, and 20, respectively. After Al_2O_3 passivation layer deposition, HfTiO gate dielectrics with thickness of 8 nm were deposited on InGaAs surface covered with Al_2O_3 interlayer by sputtering HfTiO target in Ar by high vacuum system (Shenyang Zky Technology Development Co., Ltd.). The Ar flow rate was kept at 20 SCCM. The deposition power, working pressure, and deposition temperature were kept at 80W, 1.0 Pa, and room temperature, respectively. As a reference, 8 nm HfTiO gate dielectric films was also directly deposited on as-received InGaAs wafer without Al_2O_3 passivation layer with sputtering of HfTiO target. To investigate the electrical properties, MOS capacitors were fabricated by evaporation-derived Au top electrode via shadow mask method and ohmic contact was achieved by sputtering Al on the backside of the wafer, followed by forming-gas (H_2 4% + N_2 96%) annealing (FGA) at 300° for 10 min.

2.2. Characterization. A phase-modulated SE (UVISEL Jobin-Yvon) was used to obtain the thickness and the optical constants of HfTiO films in the range of 0.75−6.5 eV with an incident angle of 70°. To interpret the measured pseudodielectric function, an optical model with three-layer-structure including InGaAs substrates, the interface layer, and a bottom bulk HfTiO layer, has been constructed. By SE analysis based on Taul−Lorentz dispersion relation for the HfTiO films, the optical constants of the HfTiO films have been determined. Additionally, ex situ X-ray photoelectron spectroscopy (XPS) measurements were carried out to study the effect of the ALD growth cycles on chemical bonding states at the MOS interfaces and the physical origins of improving the HfTiO/InGaAs MOS interface properties by introduction of Al_2O_3 passivation layer. Here, Thermo Scientific XPS ((ESCALAB 250Xi) system is equipped with Al Kα source (1486.6 eV) under base pressure of 2.1×10^{-9} Torr. The

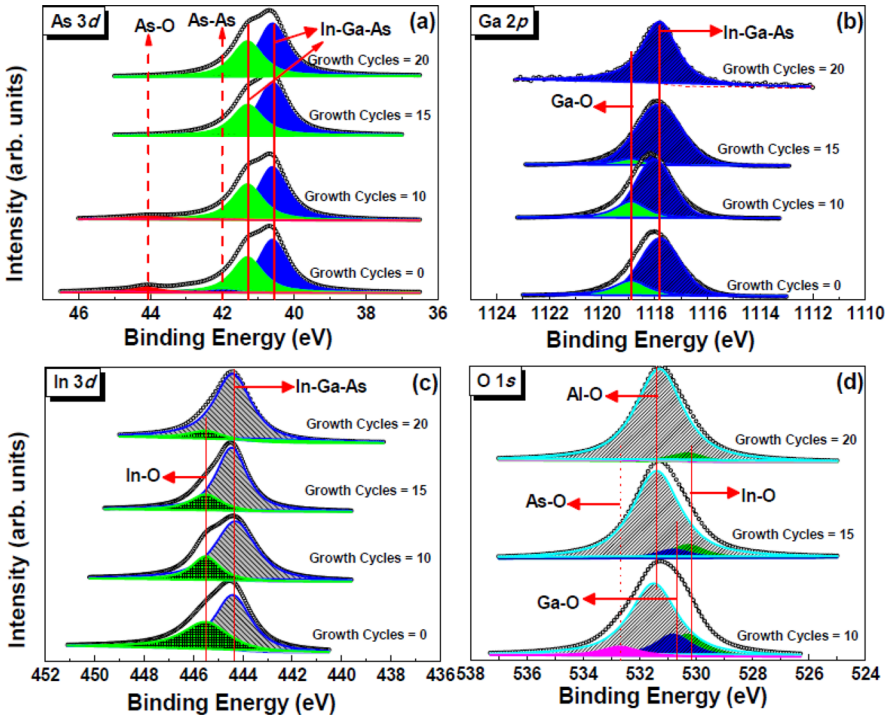

Figure 1. ALD Al_2O_3 growth cycles dependent As 3d (a), Ga 2p (b), In 3d (c), and O 1s (d) XPS core-level spectra.

source power was 150 W (15 kV × 10 mA) and the analysis region was a round spot with a radius of 500 μm. Broad band scans with pass energy of 50 eV were performed twice to acquire the binding energy of specific elements. Narrow scans with pass energy of 20 eV were performed for 20 times for binding energy of specific elements. The C 1s line with a binding energy of 284.6 eV was used as a reference to eliminate the charging effect. The charge neutralizations of X-ray bombarded samples are performed by flood guns. For the depth profiling of different atoms in gate stack, an emission angle from samples surface normal setup was changed from 0° (bulk sensitive) to 80° (surface sensitive). Spectral fitting was done by Shirley background subtraction using the Gaussian and Lorentzian functions. By characterization from XPS, the observed chemical ratio of the HfTiO film is $Hf_{0.79}Ti_{0.21}O_2$. Electrical characteristics are extracted by capacitance–voltage (C–V) measurements. An semiconductor device analyzer (Agilent B1500A) combined with Cascade Probe Station was used for C–V measurement at room temperature. Short circuit and open circuit calibration were performed before real measurements. Sinusoid signals with different frequency range of 1 kHz to 1 MHz were superimposed upon a direct current (DC) voltage, which was applied between top and bottom electrodes. And the DC voltage was swept from negative to positive or back and forth to perform single and double sweeps. Additionally, the leakage current properties were measured by B1500A. All the electrical tests were performed in a dark box.

3. RESULTS AND DISCUSSION

3.1. Interface Bonding States and Depth Profile. Previous reports have confirmed that ALD-derived Al_2O_3 has self-cleaning effect on the reduction and removal of surface oxides from GaAs or InGaAs substrate.[28,29] Such an observation has been found to be affected by oxidation state, as well as metal organic precursor.[28] Although much more attention has been paid to investigate ALD-derived high-k gate dielectric with self-cleaning effect, a key factor to determine the high-k/InGaAs interface properties has not been fully identified yet. On the basis of the references, it can be noted that chemical reactions at an InGaAs surface during the ALD process can be affected by the ALD temperature.[20,30] However, the effect of the ALD growth cycles on the interface chemistry of high-k/InGaAs has not been investigated systematically. To study the effect of Al_2O_3 ALD growth cycles on the surface chemical bonding states of InGaAs substrate, As 3d, Ga 2p, In 3d, and O 1s XPS spectra have been demonstrated in Figure 1. For the substrate prior to Al_2O_3 deposition, it can be noted that the InGaAs surface was covered with native oxides, such as AsO_x, InO_x, and GaO_x, suggesting that the surface native oxides can not be removed effectively only by surface cleaning, which act as the main source of Fermi level pinning in III–V MOSFETs devices. Therefore, removing the surface species has been confirmed to be effective in unpinning the Fermi level. Previous publications have indicated that that the native oxides from the surface of III–V wafers can be removed by some chemical solution cleaning, such as HF, HCl.[8,31] However, the remained impurity, such as F^- and Cl^-, will lead to the formation of interface layer with high density of interfacial trap states and degrade the CMOS performance. To avoid chemical impurity, ALD-derived Al_2O_3 passivation layer with self-cleaning effect has been directly deposited on InGaAs substrate. Based on the As 3d, Ga 2p, and In 3d core-level spectra demonstrated in Figure 1, it can be noted that the InGaAs surface chemistry is affected by introducing Al_2O_3 passivation layer effectively. From Figure 1a, AsO_x and As have been detected to exist at the Al_2O_3/InGaAs gate stack with growth cycles of 10. With the increase in growth cycles, reduction in native oxide has been observed. When increasing the growth cycles to 20, AsO_x has been fully removed effectively. Based on the evolution of Ga 2p core level spectra shown in Figure 1b, it can be seen that GaO_x decreases during ALD and GaO_x at the Al_2O_3/InGaAs interfaces also tends to disappear with ALD growth cycles of 20. Figure 1c shows In 3d XPS spectra from the Al_2O_3/InGaAs interfaces deposited at various growth cycles. Judging from the In 3d spectra in Figure 1c, the amount of InO_x demonstrates a slight reduction with increasing the growth cycles. However,

ALD of Al_2O_3 cannot remove InO_x native oxide fully. To confirm previous observations, O 1s XPS spectra shown in Figure 1d have been investigated. Under lower growth cycles of Al_2O_3, all the native oxides still exist. With increasing the growth cycles, the amount of AsO_x and GaO_x decreases and disappears with the growth cycles of 20. However, in spite of the reduction in amount for InO_x, the complete removal of InO_x has not been observed, confirmed by previous XPS measurements. Therefore, it can be deduced that ALD growth cycles dependence of the Al_2O_3/InGaAs interfaces would not be attributable to the existence of InO_x but to the remove of AsO_x and GaO_x. Similar trends have been found for MOCVD-deposited AlON gate dielectrics in InGaAs substrate in our previous publications.[30] The reason why the InO_x remains even increasing the ALD growth cycles or MOCVD temperature is still not clear at present. Currently, further detailed studies are needed to provide the appropriate reason in future.

Figure 2 demonstrates the Al 2p core-level spectra of as-treated InGaAs samples related to ALD growth cycles. For as-treated sample with ALD growth cycles of 10, a peak located at 74.4 eV has been detected, resulting from the AlO_x layer formed on the surface, indicating that lower growth cycles do not lead to the formation of stoichiometric Al_2O_3 layer. With the increase in growth cycles, the peak attributed to Al−O bond shifts to 74.5 and 74.8 eV for the samples with growth cycles of 15 and 20 s, respectively. Such chemical shift with increasing the growth cycles indicates the full oxidation of AlO_x layer, which is contributed to the oxygen source from the H_2O precursor and surface native oxides, leading to the reduced native oxides from the surface of InGaAs substrate. To further confirm the full oxidation of AlO_x layer and existence of InO_x native oxide at Al_2O_3/InGaAs interface with growth cycles of 20, the depth profile of Al_2O_3/InGaAs gate stack has been investigated by angle resolved XPS (ARXPS) measurement, which is a nondestructive technique and has the potential to probe subsurface chemical states. As we know, with the increase of emission angle, the probing depth becomes shallow and the surface region is probed. Therefore, by changing the emission angle, the information from the interfacial region will be detected. Figure 3 show the 2D images of Al 2p and O 1*s* spectra as a function of emission angle. For Al 2p 2D images demonstrated in Figure 3a, narrow baseline standing for Al 2p core-level spectra has been observed and no apparent difference for the Al 2p binding energy has been detected regardless of the emission angle, indicating that Al−O component is uniformly distributed in the film. On the basis of the 2D O 1s XPS spectra shown in Figure 3b, only Al−O and In−O have been detected, indicating the formation of AlO_x and InO_x component. Additionally, no GaO_x and AsO_x have been found for Al_2O_3/InGaAs gate stacks with ALD growth cycles of 20, which can be attributed to the fact that a self-cleaning effect of ALD of Al_2O_3 leads to the reduction and remove of surface oxides from InGaAs surface. Therefore, it can be inferred that ALD-derived Al_2O_3 passivation layer can serve as an oxygen reaction barrier and prevent the formation of oxide with low quality.

To investigate the effect of the ALD-derived Al_2O_3 passivation layer with growth cycles of 20 on the interface chemistry and bonding states of HfTO/InGaAs gate stacks, the evolution of the As 3d, Ga 2p, In 3d, Hf 4f, Ti 2p, and O 1s core-level spectra are demonstrated in Figure 4. For Ga 2p and

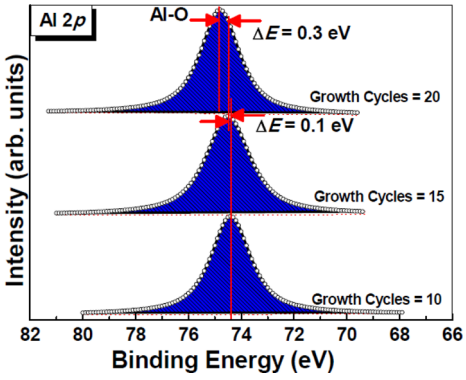

Figure 2. ALD Al_2O_3 growth cycles dependent Al 2p XPS core-level spectra.

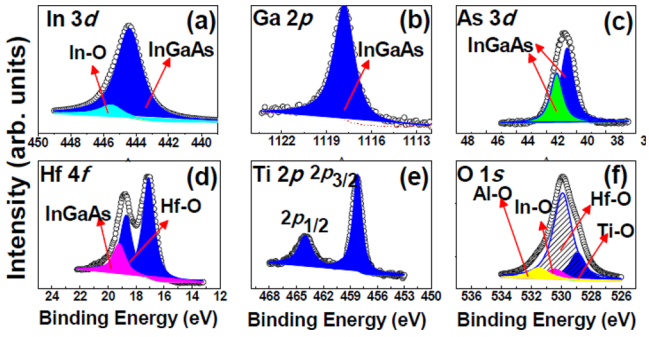

Figure 4. In 3d (a), Ga 2p (b), As 3d (c), Hf 4f (d), Ti 2p (e), and O 1s (f) XPS spectra of HfTiO/InGaAs gate stack with Al_2O_3 passivation layer.

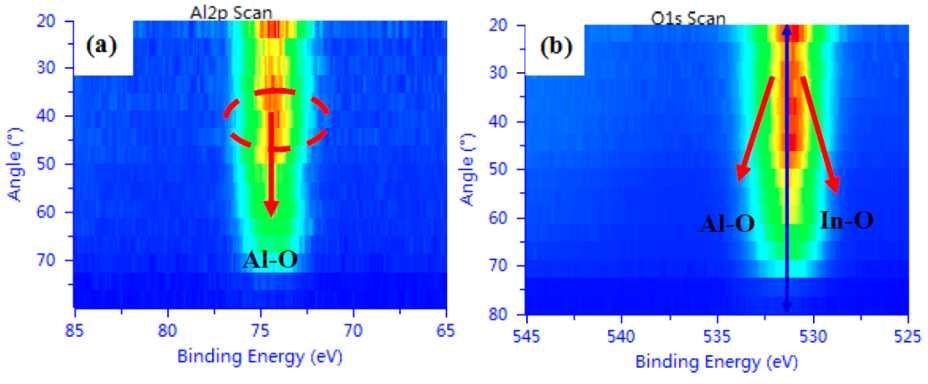

Figure 3. ARXPS 2D images of Al 2p (a) and O 1s (b) XPS spectra of Al_2O_3/InGaAs gate stacks with ALD growth cycles of 20.

As 3d spectra of HfTiO/Al_2O_3/InGaAs gate stack, demonstrated in Figure 4b and 4c, only information from InGaAs has been detected and no other oxides have been observed, suggesting that the native oxides of GaO_x and AsO_x from InGaAs surface have been effectively suppressed after deposition of Al_2O_3 passivation layer. However, for In 3d spectra displayed in Figure 4a, two deconvoluted spectra have been found. One originates from InGaAs substrate and the other is attributed to the InO_x component located at HfTiO/InGaAs interface. Based on these observations, it can be inferred that ALD-derived Al_2O_3 passivation layer with growth cycles of 20 is effective in suppressing the growth of native oxides of GaO_x and AsO_x, but no effect in removing InO_x component. Figure 4d and 4e display Hf 4f and Ti 2p core-level spectra. Comparison with the reported values of 16.2 and 17.8 eV for Hf $4f_{7/2}$ and Hf $4f_{5/2}$ peaks of HfO_2 as well as 458.3 and 464.3 eV for Ti $2p_{3/2}$ and Ti $2p_{1/2}$ peaks of TiO_2,[22,24] the binding energies for Hf 4f and Ti 2*p*, demonstrated in Figure 4d and 4e, have no shift for HfTiO samples, which can be explained by the observations from Ye et al.[32] TiO_2 addition to HfO_2 stabilizes the amorphous state of HfO_2 and both HfO_2 and TiO_2 can coexist as amorphous state in the HfTiO film and they only mixes together.[32] Because of the overlapped Hf 4f XPS spectrum with that of Ga 3d spectrum, Figure 4d also demonstrates some important information from HfTiO/InGaAs interface. The peak located at 19.2 eV is mainly attributed to the InGaAs substrate.[33] In addition, no other peak due to the Ga−O bond has been detected, suggesting no formation of native oxide at HfTiO/InGaAs interface after Al_2O_3 incorporation. To confirm the only existence of interface oxide of InO_x, O 1*s* spectra of HfTiO/InGaAs system with Al_2O_3 interlayer layer (Figure 4(f)), four deconvoluted spectra, assigned as Hf−O, Ti−O, Al−O, and In−O bonding states, respectively, have been observed. Obviously, only InO_x native oxide still exists at the interface even if the incorporation of Al_2O_3 passivation layer. Therefore, it can be concluded that ALD-derived Al_2O_3 passivation layer with growth cycles of 20 can restrain the growth of the native oxides of GaO_x and AsO_x effectively, but no effect in controlling and fully removing InO_x layer. Additionally, the remained native oxide of InO_x can not be removed by the direct deposition of HfTiO on Al_2O_3/InGaAs gate stack. The mechanics for the existence of InO_x at HfTiO/InGaAs interface is being investigated.

As a reference, the interface chemical bonding states of HfTiO/InGaAs gate stack without Al_2O_3 control layer have also been investigated. Figure 5 shows the In 3d, Ga 2p, As 3d, Hf 4f, Ti 2p, and O 1s core-level spectra from HfTiO/InGaAs interface. On the basis of the evolution of In 3d, Ga 2p, and As 3d spectra, shown in Figure 5a−c, respectively, three native oxides (GaO_x, AsO_x, and InO_x) from InGaAs surface are detected. According to previous observation, it can be noted that the existence of GaO_x can also be determined by Hf 4f spectra displayed in Figure 5d. Figure 5f demonstrates the O 1s core-level spectra of HfTiO/InGaAs system. The deconvoluted O 1s spectra show five peaks, which is assigned as Hf−O, Ti−O, Ga−O, As−O, and In−O bonding states, respectively. So, it can be inferred that direct deposition of HfTiO gate dielectric can not remove all the native oxides from InGaAs substrate.

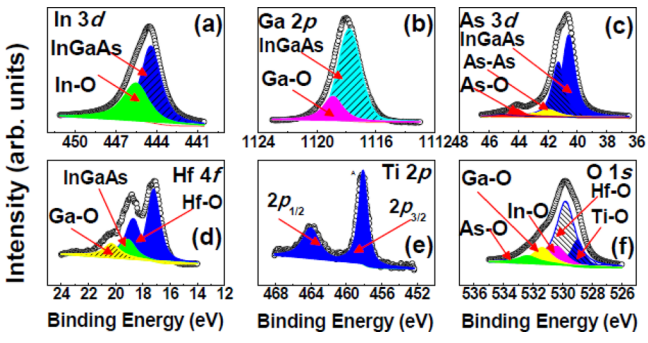

Figure 5. In 3d (a), Ga 2p (b), As 3d (c), Hf 4f (d), Ti 2p (e), and O 1s (f) XPS spectra of HfTiO/InGaAs gate stack without Al_2O_3 passivation layer.

To further confirm the change of the interfacial chemical bonding states related with Al_2O_3 passivation layer, the depth profile of HfTiO/GaAs gate stack has also been studied by ARXPS measurements. Figures 6 and 7 show the 2D images of Ga 2p, Hf 4f, O 1s, and Ti 2p XPS spectra of HfTiO/Al_2O_3/InGaAs and HfTiO/InGaAs gate stacks as a function of emission angle, respectively. For emission-dependent Ga 2p 2D images shown in Figure 7a, two different components, assigned as Ga−O and In−Ga−As bonding states, have been observed. After deposition of Al_2O_3 passivation layer, only InGaAs has been detected. Similar experimental results have been confirmed by the evolution of Hf 4f 2D images shown in Figure 6b and Figure 7b, indicating that the native oxide of GaO_x has been effectively suppressed after deposition of Al_2O_3 layer with self-cleaning effect. For Ti 2p 2D images displayed in Figure 6d and Figure 7d, no apparent emission dependent Ti 2p spectra have been found regardless of Al_2O_3 incorporation, suggesting that TiO_2 is distributed in the HfTiO film uniformly. For O 1s 2D images demonstrated in Figure c, the broadening image of the O 1s XPS spectra for HfTiO/InGaAs system indicates more components in HfTiO/InGaAs gate stack. After Al_2O_3 deposition, the O 1s 2D image displays apparent narrowing trend, suggesting the reduction of interfacial component in HfTiO/Al_2O_3/InGaAs gate stack. According to 2D ARXPS images, it can be inferred that the incorporation of Al_2O_3 passivation layer into HfTiO/InGaAs gate stack is effective in suppressing the regrowth of native oxides, which strongly supports previous observations confirmed by XPS.

3.2. Band Alignment Analysis. A major concern to use high-k gate oxide is the magnitude of the band offset (BO) between the oxide and the semiconductor. The band gaps of high-k gate dielectrics are smaller than that of SiO_2, and the band offsets between high-k materials and substrate are also smaller than those between SiO_2 and substrate. It is important to the success of MOSFET devices using high-k gate oxide that the BO between the high-k oxide and the semiconductor be at least 1 eV, as set forth by the Semiconductor Industry Association, to inhibit the flow of electrons from the semiconductor to the metal, that is, gate leakage current. A less critical factor to the success of high-k MOSFET, but still of interest, is the valence band offset (VBO) between the high-k oxide and the semiconductor. The measured offsets can be used to draw the energy-band alignment for the interface between HfTiO and InGaAs substrate.

Based on the model proposed by Kraut,[34,35] the valence band offset (ΔE_v) values of HfTiO/InGaAs and HfTiO/Al_2O_3/InGaAs gate stacks are calculated using the equation

$$\Delta E_v = (E_{As3d} - E_{VBM})_{InGaAs} - (E_{Hf4f} - E_{VBM})_{HfTiO} - (E_{As3d} - E_{Hf4f})_{HfTiO/InGaAs} \quad (1)$$

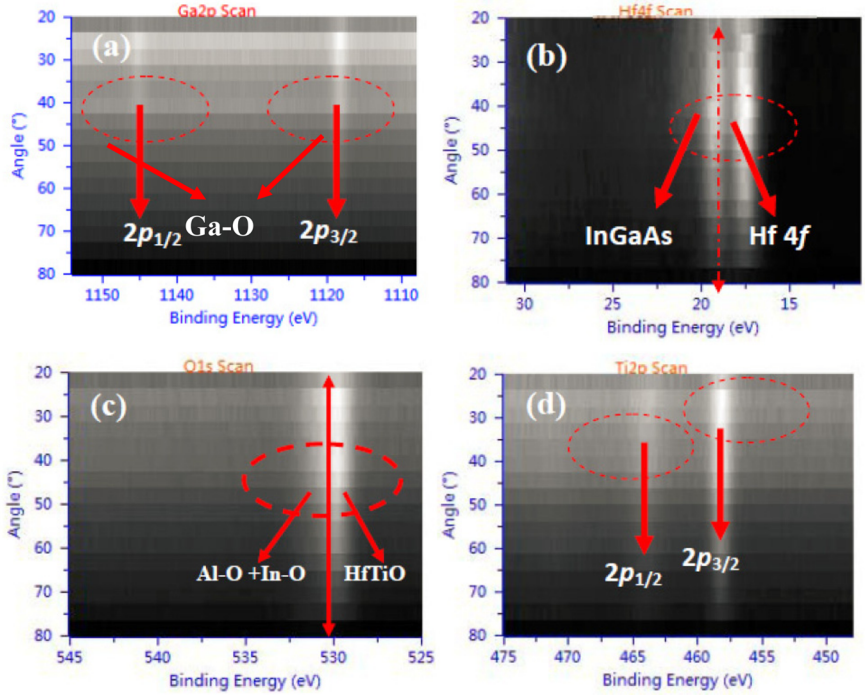

Figure 6. ARXPS 2D images of Ga 2p (a), Hf 4f (b), O 1s (c), and Ti 2p (d) XPS spectra of HfTiO/InGaAs gate stacks with Al_2O_3 passivation layer.

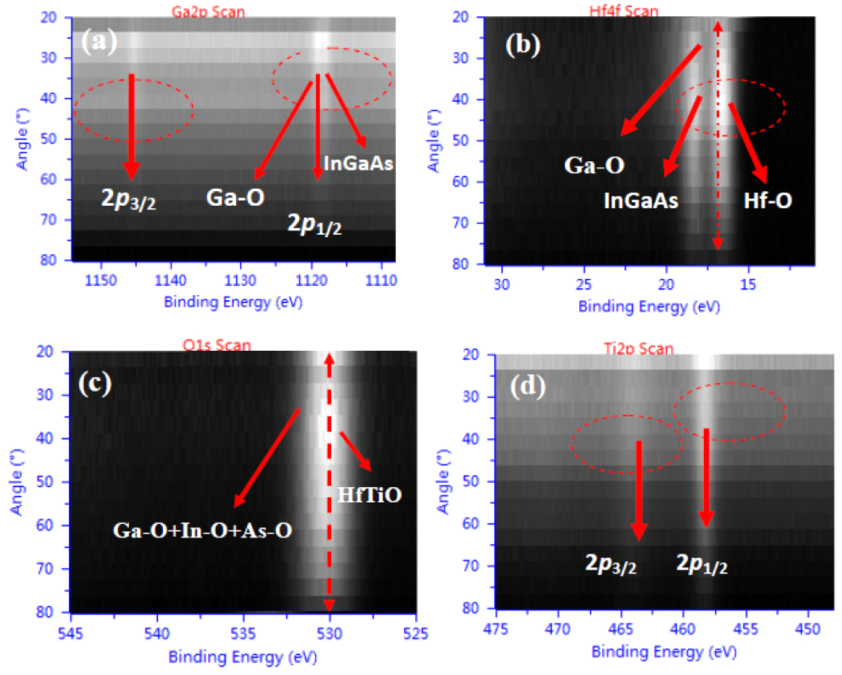

Figure 7. ARXPS 2D images of Ga 2p (a), Hf 4f (b), O 1s (c), and Ti 2p (d) XPS spectra of HfTiO/InGaAs gate stacks without Al_2O_3 passivation layer.

where E_{As3d} and E_{Hf4f} are the core level positions, E_{VBM} for InGaAs and HfTiO are the valence band maximum (VBM) of these bulk materials, combined with the core level difference of the heterojunction (HfTiO/InGaAs) with 8 nm think oxide insulators. To remove the native oxide from InGaAs, the bulk sample was etched by diluted HF to exclude the surface arsenic contribution to the reference As 3d peak.[36] The VBM values of InGaAs and 15 nm thick HfTiO were determined by extrapolating a linear fit for the leading edge of the valence band photoelectron spectra to the baseline.[37] Table 1 summarizes the core level energies and VBM values, corresponding to Figures 8 and 9. By inserting As $3d_{5/2}$, and Hf $4f_{7/2}$ binding energies and the VBM values in eq 1, the ΔE_v values for the HfTiO/Al_2O_3/InGaAs and HfTiO/InGaAs heterojunctions were calculated to be 2.43 and 2.90 eV, respectively. On the basis of Figures 8 and 9, reduction in ΔE_v has been detected for HfTiO/Al_2O_3/InGaAs gate stack. The difference in ΔE_v can mainly be due to the effect of the interfacial native oxides. The reduction in ΔE_v for HfTiO/Al_2O_3/InGaAs can be attributed to the effect of the native

Table 1. Summary of Core Levels, Valence Bands, Conduction Band Offsets ΔE_c, and Valence Band Offsets ΔE_v for Bulk *n*-Type InGaAs, and HfTiO Films on *n*-Type InGaAs with and without Al_2O_3 Passivation Layer

sample	$E_{As3d5/2}$ (eV)	$E_{Hf4f7/2}$(eV)	E_{VBM} (eV)	ΔE_v (eV)	ΔE_c (eV)
bulk clean InGaAs	40.86		0.60		
15 nm HfTiO/InGaAs		17.51	3.36	2.90	1.76
15 nm HfTiO/Al_2O_3/InGaAs		17.45	3.63	2.43	2.23
8 nm HfTiO/InGaAs	40.74	17.06			
8 nm HfTiO/Al_2O_3/InGaAs	40.70	17.16			

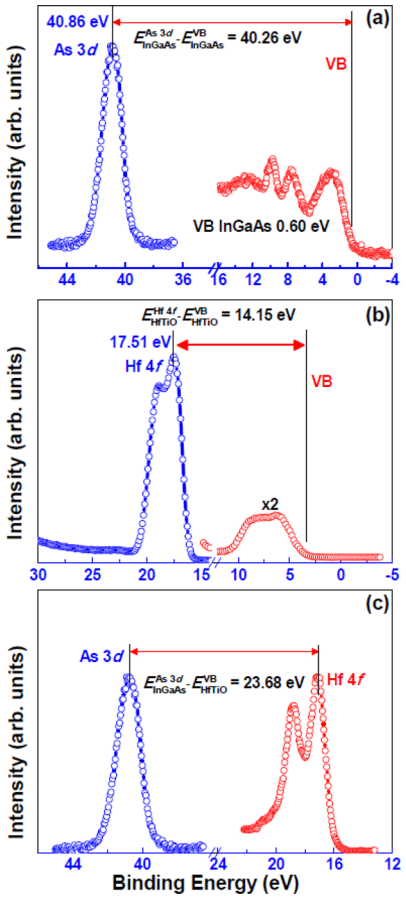

Figure 8. XPS spectra of (a) As 3d core level and valence band of InGaAs film, (b) Hf 4f core level and valence band of HfTiO film, and (c) As 3d and Hf 4f core levels at the HfTiO/Al_2O_3/InGaAs interface.

oxides located at HfTiO/InGaAs interface, which is consistent with the Robertson' observation that the band offset of high-*k*/high mobility substrates can be increased by the existed interfacial layer.[38]

To determine the conduction band offset (ΔE_c) values of the HfTiO/InGaAs and HfTiO/Al_2O_3/InGaAs gate stacks, the band gap energy E_g of HfTiO was obtained by UV−vis measurements. By extrapolating the linear portion of the curves relating $(\alpha h\nu)^{1/2}$ and hν to $(\alpha h\nu)^{1/2} = 0$ ($h\nu$ is the photon energy and α is the absorption coefficient), band gap energy of 5.54 eV for HfTiO gate dielectric film has been decided.

ΔE_c can be achieved by subtracting ΔE_v and the energy gap of the InGaAs substrate and HfTiO film, as expressed in following equation

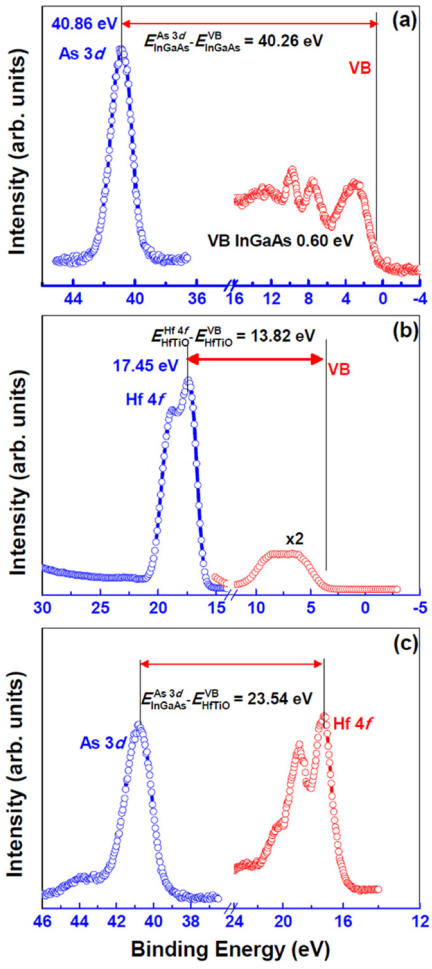

Figure 9. XPS spectra of (a) As 3d core level and valence band of InGaAs substrate, (b) Hf 4f core level and valence band of HfTiO film, and (c) As 3d and Hf 4f core levels at the HfTiO/InGaAs interface without Al_2O_3 passivation layer.

$$\Delta E_c(\mathrm{HfTiO} - \mathrm{InGaAs}) = E_g(\mathrm{HfTiO}) - \Delta E_v(\mathrm{HfTiO} - \mathrm{InGaAs}) - E_g(\mathrm{InGaAs}) \quad (2)$$

where E_g(HfTiO) is the band gap of HfTiO and E_g(InGaAs) is the band gap of InGaAs substrate. Taking into account the measured energy-band gap of sputtering-deposited HfTiO (5.40 eV), and together with the InGaAs energy-band gap as 0.74 eV,[39] the ΔE_c of 2.23 eV is deduced with Al_2O_3 passivation layer whereas 1.76 eV without Al_2O_3 passivation layer. Increased ΔE_c has been observed after Al_2O_3 incorporation, resulting from the suppressed interfacial layer. For high-*k* gate dielectrics, the asymmetric band alignments will lead to larger leakage current.[40] In our case, the sputtered HfTiO gate dielectric brings about near-symmetric band alignment and large band offset over 1 eV and make HfTiO/InGaAs gate stacks with Al_2O_3 passivation layer suitable for the fabrication of MOSFETs with small leakage current induced by Schottky emission.[41] However, compared to the reported ΔE_c of 1.97 eV for *p*-InGaAs/HfAlO, the lowering of the ΔE_c in HfTiO/Al_2O_3/InGaAs gate stack may be due to the smaller band gap of HfTiO dielectrics.[24] Therefore, TiO_2 component in HfTiO should be systematically modulated to ensure improved

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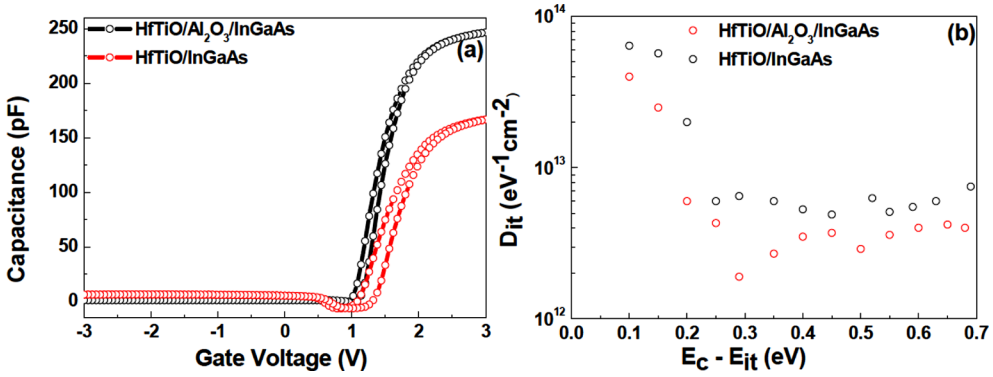

Figure 10. (a) $C-V$ (a) characteristics of InGaAs-based MOS capacitors with and without Al_2O_3 incorporation. (b) Energy distributions of D_{it} for Au/HfTiO/InGaAs MOS capacitors with and without Al_2O_3 passivation layer.

Table 2. Parameters of the InGaAs MOS Capacitors with and without Al_2O_3 Passivation Layer Extracted from HF $C-V$ Curves[a]

MOS capacitor	dielectric constant	flat band voltage (V)	leakage current density (A/cm^2)	frequency dispersion (%)	interface state density (eV^{-1} cm^{-2})	oxide-charge density (cm^{-2})
HfTiO/InGaAs	18.7	1.42	1.26×10^{-4}	30.9	6.0×10^{12}	-6.5×10^{13}
$HfTiO/Al_2O_3/InGaAs$	21.8	1.21	1.17×10^{-5}	3.52	1.9×10^{12}	-8.5×10^{12}
$HfO_2/Gd_2O_3/GaAs$[47]		−0.7		8.5	4×10^{12}	
$ZrO_2/Si/GaAs$[48]	12	−0.45			5×10^{12}	
$TiO_2/AlON/GaAs$[49]	22	0.6	2.8×10^{-5}		6.9×10^{12}	3.5×10^{12}
$HfO_xN_y/GaAs$[50]	24	−0.6	6.9×10^{-6}			
$(TiO_2)_x(Al_2O_3)_{1-x}/In_{0.53}Ga_{0.47}As$[51]			$5-9 \times 10^{-7}$	11	4.2×10^{11}	
HfAlO/GaAs[52]	7.5		$2-5 \times 10^{-6}$		8×10^{11}	

[a]For comparison, reported data on high-k/GaAs and high-k/InGaAs with and without passivation layer are also concluded together.

electrical properties of $HfTiO/Al_2O_3/InGaAs$ gate stacks in MOSEFETs devices.

3.3. Electrical Analysis. High frequency (1 MHz) $C-V$ characteristics of n-InGaAs MOS capacitors with and without Al_2O_3 control layer has been displayed in Figure 10a. For HfTiO/InGaAs sample, the curves stretched out along the voltage axis suggesting the formation of high density of defective states at the conduction-band edge of InGaAs caused by a considerable amount of As−O, As−As, and Ga−O bonds at the HfTiON/InGaAs interface.[26,42,43] However, the "stretched out" effect has been observed to disappear when Al_2O_3 passivation layer has been introduced before high-k gate dielectrics deposition, which can be attributed to the improved interfacial properties. On the basis of Figure 10a, it can be noted that HfTiO/InGaAs sample with Al_2O_3 passivation layer demonstrates a smaller hysteresis voltage than that of HfTiO/InGaAs sample without Al_2O_3 passivation layer, implying fewer slow states in the dielectric and near/at the interface due to the reduction of Ga and As diffusions in the sample with Al_2O_3 passivation layer.[44] For HfTiO/InGaAs gate stack, the $C-V$ curve displays an accumulation region at higher positive voltages attributed to the steady-state nonequilibrium conditions for semiconductors with wide band gap.[44] However, for $HfTiO/Al_2O_3/InGaAs$ system, the accumulation and the depletion regions are detected, suggesting that the introduced Al_2O_3 control layer prevents the formation of gallium and arsenic oxides and thus the generation of surface states from the interface has been controlled. The suppression of the formation of low-k interface layer leads to high accumulation capacitance compared to directly deposited HfTiO. For the $HfTiO/Al_2O_3/InGaAs$ gate stack, the suppressed formation of low-k interface layer eventually leads to unpinned Fermi level and good interface properties. In addition, the extracted positive flat band voltage (V_{FB}) from the $C-V$ curves suggests that the existed native defects/traps in the samples are negative. For the sample without Al_2O_3 passivation layer, $HfTiO/Al_2O_3/InGaAs$ gate stack displays smaller positive V_{FB} shift, indicating the less negative oxide charges, which can be attributed to either singly and doubly negatively charged interstitial oxygen atoms,[45] or reduction of defect traps in the film and near the interface.[46] The equivalent k value, V_{FB}, density of oxide charge (Q_{ox}), including the oxide charges, mobile-ion charges, border-trap charges, and interface-state charges of the HfTiO/InGaAs and $HfTiO/Al_2O_3/InGaAs$ gate stacks were obtained from $C-V$ curves with high frequency, as listed in Table 2. As a comparative study, some reported results have been included in Table 2. Because of the suppressed interfacial layer, $HfTiO/Al_2O_3/GaAs$ achieves the larger equivalent k value of 21.8. The negative Q_{ox} could be related with acceptor-like interface and near-interface traps.[44,53] Border traps are the near interfacial oxide traps that can slowly or rapidly exchange charge with the substrate and can look either like interface traps or like bulk oxide traps depending on the bias, voltage ramp rate and measurement frequency. The densities of both border traps (N_{bt}) and interface states (D_{it}) were determined to characterize the interface properties. The border trap charges were determined from high frequency (1 MHz) $C-V$ hysteresis measurements. From the hysteresis, border trap density ($N_{bt} = C_{ox}\Delta V_{mg}/Aq$) was calculated. For samples with Al_2O_3 passivation layer, it was found to be 2.6×10^{12} cm^{-2}. For MOS capacitors without Al_2O_3 layer, the value was 7.8×10^{12} cm^{-2}. The improved interface quality is also confirmed by energy distribution of density of interface state (D_{it}) in the bandgap as shown in Figure 10b, which is extracted from $C-V$

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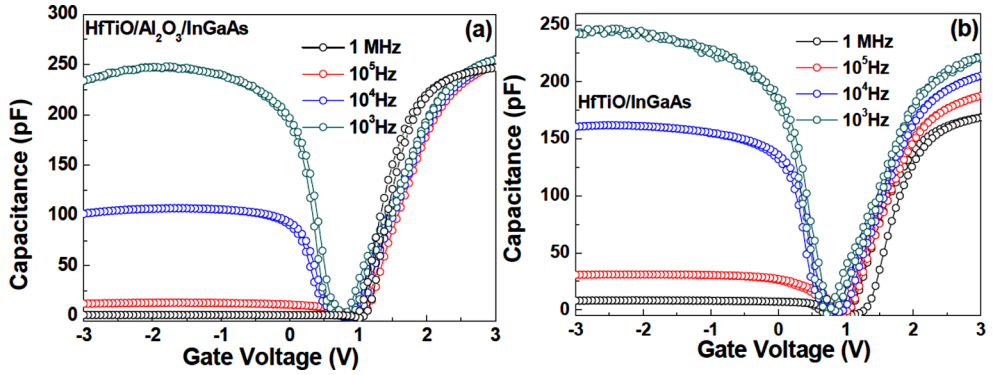

Figure 11. $C-V$ characteristics at different frequencies ranging from 1 kHz to 1 MHz: (a) Au/HfTiO/Al_2O_3/InGaAs and (b) Au/HfTiO/InGaAs MOS capacitors.

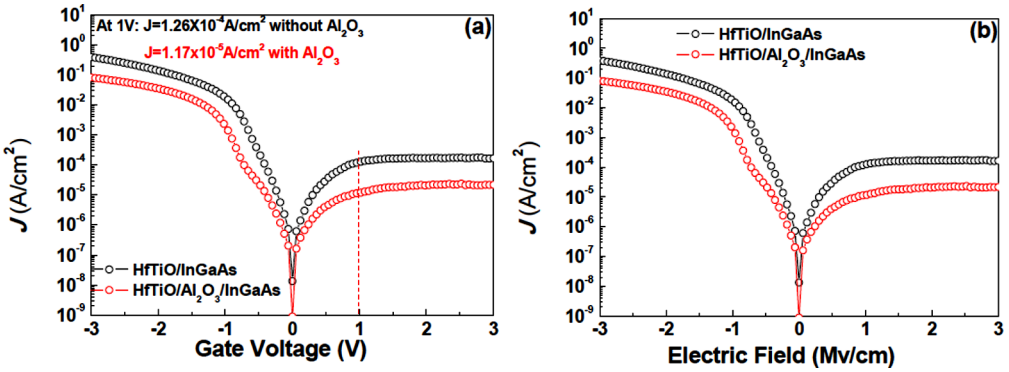

Figure 12. (a) $J-V$ and (b) $J-E$ characteristics of InGaAs-based MOS capacitors with and without Al_2O_3 passivation layer.

curve of the two samples by using the Terman's method.[54] On the basis of Figure 10b, it can be noted that the interface trap density of Au/HfTiO/Al_2O_3/InGaAs MOS capacitor is lower than that of sample without Al_2O_3 passivation layer, indicating that the introduced Al_2O_3 control layer can effectively reduce the interface trap density and improve the interfacial properties of HfTiO/InGaAs gate stack. The D_{it} for MOS capacitor with Al_2O_3 layer is calculated to be 1.9×10^{12} cm^{-2} V^{-1}, while the value of D_{it} for MOS capacitor without Al_2O_3 control layer is 6.0×10^{12} $cm^{-2}eV^{-1}$. In comparison, the D_{it} from $Ga_2O_3(Gd_2O_3)/In_{0.15}Ga_{0.85}As$ is at least 1 order of magnitude lower in the range less than 10^{11} $cm^{-2}eV^{-1}$.[55] The higher D_{it} in HfTiO/Al_2O_3/InGaAs can be attributed to the existence of In_2O_3 at the interface, while there are no such native oxides at $Ga_2O_3(Gd_2O_3)$/InGaAs interfaces.[49,55] On the basis of previous observations, it can be concluded that the introduced Al_2O_3 passivation layer attributes to the formation of HfTiO/InGaAs interface with high quality by reducing interface states and border traps and thus unpin the Fermi level.

Figure 11a and b show the $C-V$ characteristics of Au/HfTiO/InGaAs and Au/HfTiO/Al_2O_3/InGaAs MOS capacitors measured at frequencies ranging from 1MH to and 1 kHz. The frequency dispersion of the accumulation capacitance is more prominent for capacitors without Al_2O_3 passivation layer. Based on the fact that the percentage frequency dispersion is defined as $[C_{1k}/C_{1M} - 1] \times 100\%$ with the capacitance value at 3 V,[56] frequency dispersion of two different MOS capacitors were found to be 3.52% and 30.9%, respectively. The frequency dependence on the Al_2O_3 passivation layer can be due to the presence of midgap states and high midgap interface state density. The D_{it} problem is more severe for HfTiO/InGaAs gate stack than that of HfTiO/Al_2O_3/GaAs. Presence of interfacial Ga_2O_3, In_2O_3, and As_2O_3 for HfTiO/GaAs gate stack creates defect levels close to the conduction band and the associated high trap density severely and contributes to the much larger frequency dispersion. Therefore, it can be concluded that the introduced Al_2O_3 passivation layer can unpin the Fermi level by suppressing the formation of surface states at the interface, confirmed by previous XPS measurements. Based on Figure 11, it can be noted that bumps in the $C-V$ curves in the depletion region regardless of Al_2O_3 passivation layer have been observed, which can be interpreted by the relationship $T_R \propto T_T/N_i$, where T_T is the lifetime of minority carrier, N_i is the intrinsic concentration, and T_R is the response time of minority carrier.[57] Because at room temperature N_i for Si is about 2 orders of magnitude lower than that in InGaAs. Therefore, T_R of InGaAs is estimated to 4 orders of magnitude smaller than that of Si.[58] Because of the shorter response time for InGaAs, an inversion layer is quickly formed in response to a higher external ac signal at the gate, namely, a high capacitance equal to C_{ox}, will be formed at frequencies as low as 1 kHz.

Figure 12a shows the current density–voltage ($J-V$) characteristics for Au/HfTiO/InGaAs and Au/HfTiO/Al_2O_3/InGaAs samples. Leakage current densities of 1.17×10^{-5} and 1.26×10^{-4}A cm^{-2} are observed for HfTiO/Al_2O_3/InGaAs and HfTiO/InGaAs gate stacks, respectively. The larger leakage current in HfTiO/InGaAs sample can result from the interface trap-assisted tunneling because interface states with high density exist at high-k/InGaAs interface of the unpassivated samples.[59] In addition, reduction in leakage current density for sample with Al_2O_3 layer may be attributed to the reduced oxide charge density and decreased interfacial defect density. At a moderate or high oxide electric field, the energy levels of some

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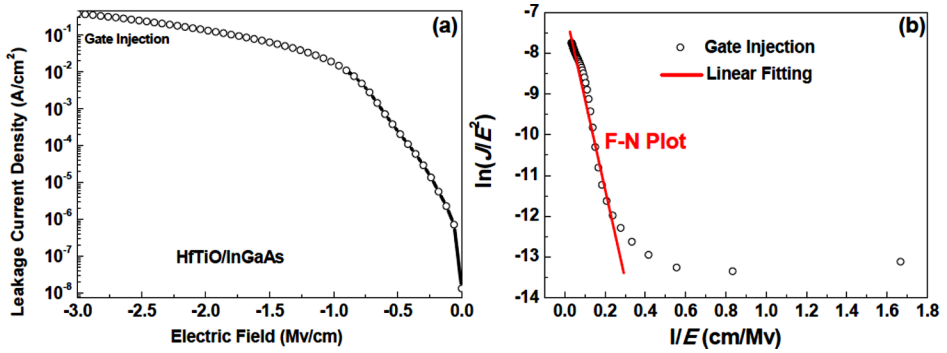

Figure 13. *J*–*E* curve of the Au/HfTiO/InGaAs/Si MOS structure (a). Conduction mechanism fitting of the MOS structure under gate injection (b).

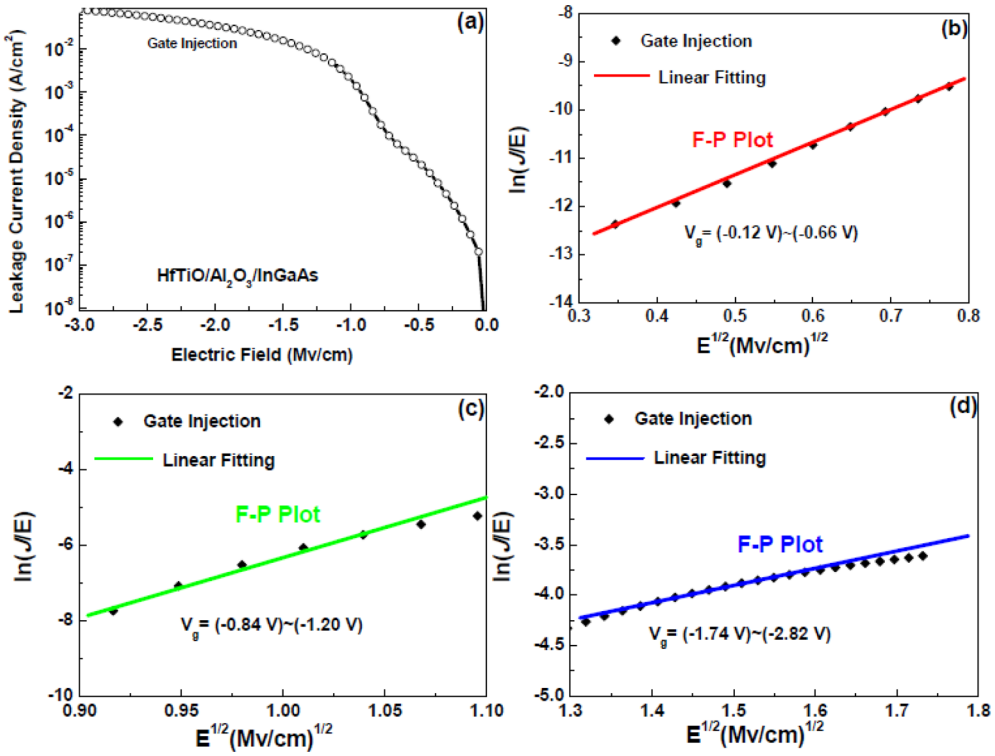

Figure 14. (a) *J*–*E* curve of the Au/HfTiO/Al_2O_3/InGaAs/Si MOS structure (a). (b, c, and d) Conduction mechanism fitting of the MOS structure under gate injection.

traps in the HfTiO dielectric are lowered to below Fermi level of the gate, and thus these traps become effective centers to generate the trap-assisted tunneling current.[60] In addition, the reduction of conduction-band offset between HfTiO and InGaAs attributed to the interfacial Ga-/As-oxides is another possible reason.[61] In other words, it can be inferred that the incorporation of Al_2O_3 passivation layer suppresses the interfacial layer growth, and results in the larger accumulation capacitance, the reduced interface states related with oxygen vacancies, or the increased conduction band offset, leading to the reduced trap-assisted tunneling current. Leakage current densities (J) of samples with and without Al_2O_3 passivation layer are depicted as a function of applied electric field (E) in Figure 12b. The asymmetry in the *J*–*E* curve results from the difference in material properties and the conduction mechanisms across the metal/high-k and high-k/substrate interfaces.[62,63]

To investigate the leakage current conduction mechanisms for InGaAs-based MOS devices with and without Al_2O_3 passivation layer, we have investigated many current conduction mechanisms (CMs), including Poole–Frenkel (F–P), Schottky emission (SE), and Fowler–Nordheim (F–N).Various CMs can occur at various electrical fields. As a result, it is not easy to fully understand and determine the exact current CMs for the SE, the PF, and the F–N mechanisms. In current work, gate injection (negative voltage on the top electrode) case has been investigated to evaluate the *J*–*V* results.

For the device without Al_2O_3 passivation layer, FN tunneling mechanism can be utilized to explain the current transport of the MOS device. F–N conduction mechanism is governed by[64]

$$J = AE^2 \exp(-B/E) \tag{3}$$

where A and B are constant and E is the electric field across the HfTiO layer. The electrical data are replotted in the form of $\ln(J/E^2)$ versus $1/E$. As shown in Figure 13b, a linear region at

high E has been observed. The linear relation of $\ln(J/E^2)$ vs $1/E$ suggests a FN tunneling through the oxide layer. Such phenomenon has been detected by from Hong et al. for ALD-derived HfO_2 on InGaAs.[51] According to the slope of the linear region, the barrier height, Φ_B, of 2.35 eV, with respect to the conduction band offset between Al_2O_3 and InGaAs, has been obtained.

For the device with Al_2O_3 passivation layer, it is evident from Figure 14 that at low-electrical fields (−0.12 to −0.55 V), medium-electrical fields (−0.84 to −1.20 V), and high-electrical fields (−1.74 to −2.82 V), J_g through the HfTiO layer is attributed to the Frenkel−Pool (F−P) conduction governed by the formula[64]

$$J = CE \exp\{[-q(\Phi_{trap} - (qE/\varepsilon_0 k_r \pi)^{1/2})/kT\} \quad (4)$$

where Φ_{trap} is the trap energy level, E is the electrical field, k_r is the permittivity, k is Boltzmann constant, T is the absolute temperature. From the slope of the plots, k_r has been extracted. Under condition of room temperature, the extracted k_r for HfTiO (20−22) are comparable to that calculated from previous $C-V$ curve. The different carrier transport mechanism suggests that Al_2O_3 passivation layer is effective in reducing the trap/defect density, and therefore significantly decreasing the leakage current density.

4. CONCLUSIONS

In current work, the effect of the growth cycles of ALD-derived Al_2O_3 passivation layer on the interface chemistry and electrical properties of MOS capacitors fabricated using sputtering-derived HfTiO as the dielectric on InGaAs has been investigated to reduce the density of interface states and avoid Fermi level pinning at HfTiO/InGaAs interface. On the basis of the comparative study on the interfacial properties of HfTiO/InGaAs and HfTiO/Al_2O_3/InGaAs gate stacks, effective passivation of InGaAs surfaces and suppression of interfacial layer with ALD-derived Al_2O_3 interface control layer confirmed by ARXPS measurements has been demonstrated. Meanwhile, reduced valence band offset and increased conduction band offset have been detected for HfTiO/Al_2O_3/GaAs gate stack. Based on high frequency (1 MHz) $C-V$ characterization, effective dielectric constants for HfTiO in HfTiO/InGaAs and HfTiO/Al_2O_3/InGaAs gate stacks are calculated to be 18.7 and 21.8, respectively. Improved frequency dispersion (~3.52%) characteristics are achieved after the introduction of Al_2O_3 passivation layer. A midgap interface state density of (~1.9) × 10^{12} eV^{-1} cm^{-2} and a low border trap density of 2.6 × 10^{12} cm^{-2} were found for HfTiO/Al_2O_3/InGaAs gate stack. The conduction mechanism for Au/HfTiO/Al_2O_3/InGaAs is dominated by Pool−Frenkel emission at gate injection case. However, for the device without Al_2O_3 passivation layer, $F-N$ dominates the conduction mechanism at higher electric field for the gate injection. In general, Al_2O_3 control layer between InGaAs and HfTiO provides a good way to passivate InGaAs surface and improve the interface quality.

■ ASSOCIATED CONTENT

Supporting Information

Comparative $C-V$ and $J-V$ characteristics of InGaAs-based MOS capacitors with different gate stacks and extracted electrical parameters from the HfO_2/InGaAs, HfTiO/InGaAs, and HfTiO/Al_2O_3/InGaAs MOS capacitors, respectively. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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